IN THE CLAIMS

We claim:

1. A circuit comprising:

at least one access device, the at least one access device comprised of a non-planar transistor having a single fin;

at least one pull-up device, the at least one pull-up device comprised of a non-planar transistor having a single fin; and

at least one pull-down device, the at least one pull-down device comprised of a non-planar transistor having multiple fins.

2. The circuit of claim 1, wherein the at least one pull-down device is comprised of a non-planar tri-gate transistor having two fins.

3. The circuit of claim 2, wherein the two fins of the non-planar tri-gate transistor are located less than 60 nm from each other.

4. A CMOS SRAM cell comprising:

two access devices, each access device comprised of a tri-gate transistor having a single fin;

two pull-up devices, each pull-up device comprised of a tri-gate transistor having a single fin;

two pull-down devices, each pull-down device comprised of a tri-gate transistor having multiple fins; and

wherein the CMOS SRAM cell has a cell ratio, a static noise margin (SNM), and a supply voltage.

5. The CMOS SRAM cell of claim 4, wherein each pull-down device is comprised of a tri-gate transistor having two fins, each fin having a height and a width.

6. The CMOS SRAM cell of claim 5, wherein the fins are located less than 60 nm from each other.

7. The CMOS SRAM cell of claim 5, wherein the height of each fin is 60 nm.

8. The CMOS SRAM cell of claim 5, wherein the width of each fin is 60 nm.

9. The CMOS SRAM cell of claim 4, wherein each tri-gate transistor contains at least one corner, each corner having a radius of curvature of less than 10 nm.

10. The CMOS SRAM cell of claim 4, wherein the cell ratio is greater than 2.0.

11. The CMOS SRAM cell of claim 4, wherein the static noise margin (SNM) is greater than 240 mV.

12. The CMOS SRAM cell of claim 11, wherein the supply voltage is less than 1.5 V.

13. A CMOS SRAM cell comprising:

two N-type access devices, each N-type access device comprised of a tri-gate transistor having a single fin;

two P-type pull-up devices, each P-type pull-up device comprised of a tri-gate transistor having a single fin;

two N-type pull-down devices, each N-type pull-down device comprised of a tri-gate transistor having multiple fins.

14. The CMOS SRAM cell of claim 13, wherein each N-type pull-down device is comprised of a tri-gate transistor having two fins, each fin having a height and a width.

15. The CMOS SRAM cell of claim 14, wherein the fins are located less than 60 nm from each other.

16. A method of forming a six transistor (6T) CMOS SRAM cell, comprising:

forming two N-type access devices, each N-type access device comprised of a tri-gate transistor having a single fin;

forming two P-type pull-up devices, each P-type pull-up device comprised of a tri-gate transistor having a single fin;

forming two N-type pull-down devices, each N-type pull-down device comprised of a tri-gate transistor having at least two fins.

17. A method of forming a semiconductor device, comprising:

forming a silicon film on a substrate;

forming a sacrificial block on the silicon film, the sacrificial block having laterally opposite sidewalls;

depositing an insulating layer over the sacrificial block and the silicon film;

forming an insulating spacer on each of the laterally opposite sidewalls of the nitride block by performing an anisotropic etch on the insulating layer;

removing the sacrificial block;

forming two silicon fins by etching through the silicon film to the substrate using the insulating spacers as a mask, wherein each silicon fin has a top surface and a pair of laterally opposite sidewalls; and

removing the insulating spacers to expose the top surface of each silicon fin.

18. The method of claim 17, wherein the substrate is an insulating substrate.

19. The method of claim 17, wherein the insulating layer is comprised of an oxide layer.

20. The method of claim 17, wherein the thickness of the silicon film is 60 nm.

21. The method of claim 17, wherein the laterally opposite sidewalls of the sacrificial block are 60 nm apart.

22. The method of claim 17, wherein the sacrificial block is defined by lithography.

23. The method of claim 18, wherein the sacrificial block is comprised of nitride.

24. The method of claim 17, wherein the thickness of the insulating layer is between 40 and 80 nm.

25. The method of claim 17, wherein the thickness of the insulating layer is 60 nm.

26. The method of claim 17, wherein the two silicon fins are separated by a distance of 60 nm or less.

27. The method of claim 17, further comprising forming a gate dielectric layer on the top surface and on the sidewalls of each silicon fin.

28. The method of claim 27, wherein the gate dielectric layer is formed by atomic layer deposition (ALD).

29. The method of claim 28, wherein each silicon fin has at least one corner having a radius of curvature, the radius of curvature being defined by the atomic layer deposition of the gate dielectric layer.

30. The method of claim 29, wherein the radius of curvature is less than 10 nm.

31. The method of claim 27, further comprising depositing a gate material over the top surface and sidewalls of each silicon fin and over the insulating substrate.

32. The method of claim 31, further comprising patterning the gate material to form a gate electrode on the gate dielectric layer.

33. The method of claim 32, further comprising forming a pair of source/drain regions in each silicon fin on opposite sides of the gate electrode.